

What is claimed is:

- 1 1. A parallel execution processor comprising:
2 a plurality of processing elements;
3 an obtaining unit operable to obtain (i) a piece of group
4 number information indicating how many groups the processing
5 elements should be formed into and (ii) an instruction sequence
6 including one or more instructions;
7 a decoding unit operable to decode the obtained instruction
8 sequence;
9 a group forming unit operable to form the processing
10 elements into as many groups as indicated by the piece of group
11 number information; and
12 an execution controlling unit operable to assign part or
13 all of the instructions included in the decoded instruction
14 sequence to the groups, so that one group receives one instruction,
15 and control the processing elements so that (i) the instructions
16 received by the groups are executed in parallel, and (ii) in
17 each group, all processing elements in the group are employed
18 in parallel for the execution of the received instruction.
- 1 2. The parallel execution processor of Claim 1, wherein
2 the instruction sequence includes as many instructions
3 as the number of groups indicated by the piece of group number

4 information.

1 3. The parallel execution processor of Claim 2, wherein
2 the number of groups indicated by the piece of group number
3 information is either one or two,
4 when the number of groups indicated is one, the group
5 forming unit forms all of the processing elements into one group,
6 and
7 when the number of groups indicated is two, the group
8 forming unit forms all of the processing elements into two groups
9 so that the two groups contain an equal number of processing
10 elements.

1 4. The parallel execution processor of Claim 3, further
2 comprising
3 a register that includes a plurality of register files
4 each of which corresponds to a different one of the processing
5 elements, wherein
6 the instruction sequence includes a first instruction and
7 a second instruction,
8 the register files are arranged in the register so that
9 first-group register files and second-group register files
10 alternate, (i) the first-group register files each storing
11 therein a piece of data to be processed when the first instruction

12 is executed and (ii) the second-group register files each storing
13 therein a piece of data to be processed when the second instruction
14 is executed,

15 when the number of groups indicated is two, the group
16 forming unit forms the processing elements corresponding to the
17 first-group register files into one of the two groups, and the
18 processing elements corresponding to the second-group register
19 files into the other group, and

20 each of the processing elements obtains the piece of data
21 to be processed from the corresponding register file.

1 5. The parallel execution processor of Claim 4, wherein
2 the register files are formed into a plurality of pairs,
3 keeping an order in which the register files are arranged in
4 the register,

5 each of the instructions includes a piece of selection
6 information indicating which piece of data, each processing
7 element should obtain, selecting out of (a) the piece of data
8 stored in the corresponding register file and (b) the piece of
9 data stored in a register file with which the corresponding
10 register file is paired, and

11 each of the processing elements obtains the piece of data
12 to be processed from the register file indicated in each piece
13 of selection information.

1 6. The parallel execution processor of Claim 3, wherein
2 when the number of groups indicated is two, the execution
3 controlling unit includes:

4 a storing unit that stores therein a plurality of
5 combination options based on which of the processing elements
6 should belong to each of the two groups, the combination options
7 being prepared for each of a plurality of grouping procedures;

8 a grouping information obtaining unit operable to
9 obtain a piece of grouping information indicating which one of
10 the grouping procedures should be used; and

11 a selecting unit operable to select one of the
12 combination options according to the obtained piece of grouping
13 information.

1 7. The parallel execution processor of Claim 3, wherein
2 when the number of groups indicated is two, the execution
3 controlling unit includes:

4 a grouping information obtaining unit operable to
5 obtain a piece of grouping information indicating to which one
6 of the two groups, each of the processing elements should belong;
7 and

8 a grouping unit operable to form the processing
9 elements into the two groups according to the obtained piece
10 of grouping information.

1 8. The parallel execution processor of Claim 1, further
2 comprising
3 a fetching unit operable to fetch a piece of data which
4 is of a predetermined length and has a format field and a data
5 field, wherein
6 each of the instructions includes an OP code and an operand,
7 a positioning pattern is written in the format field, the
8 positioning pattern being for positioning OP codes and operands
9 in the data field,
10 in the piece of data, one or more OP codes and one or more
11 operands are arranged in the data field in an order defined by
12 the positioning pattern written in the format field,
13 the number of groups indicated by the piece of group number
14 information is a number of instructions defined by the
15 positioning pattern,
16 the decoding unit extracts, from the piece of data, the
17 one or more OP codes and the one or more operands, according
18 to the positioning pattern so as to decode the OP codes and the
19 operands of the instructions, and
20 the execution controlling unit assigns, in the defined
21 order, the decoded instructions to the groups.

1 9. The parallel execution processor of Claim 1, further
2 comprising:

3 a fetching unit operable to fetch a piece of data which
4 is of a predetermined length; and
5 a storing unit operable to store therein a predetermined
6 positioning pattern for OP codes and operands, wherein
7 each of the instructions includes an OP code and an operand,
8 one or more OP codes and one or more operands are arranged
9 in the piece of data in an order defined by the predetermined
10 positioning pattern,
11 the number of groups indicated by the piece of group number
12 information is a number of instructions defined by the
13 positioning pattern,
14 the decoding unit extracts, from the piece of data, the
15 one or more OP codes and the one or more operands, according
16 to the positioning pattern so as to decode the OP codes and the
17 operands of the instructions, and
18 the execution controlling unit assigns, in the defined
19 order, the decoded instructions to the groups.

1 10. The parallel execution processor of Claim 1, wherein
2 when the number of groups indicated by the piece of group
3 number information is two or larger, the obtaining unit obtains
4 an instruction that instructs that processing elements included
5 in some of the groups should halt operation, and
6 the execution controlling unit controls the processing

7 elements included in those groups so that those processing
8 elements halt operation.

1 11. A parallel execution processor comprising:
2 a plurality of processing elements;
3 a register that includes a plurality of register files
4 each of which corresponds to a different one of the processing
5 elements, the register files being arranged in the register so
6 that first-group register files and second-group register files
7 are positioned according to a predetermined rule, (i) the
8 first-group register files each storing therein a piece of data
9 to be processed when a first instruction is executed and (ii)
10 the second-group register files each storing therein a piece
11 of data to be processed when a second instruction is executed;
12 an obtaining unit operable to obtain an instruction
13 sequence that includes the first instruction and the second
14 instruction;
15 a decoding unit operable to decode the first instruction
16 and the second instruction included in the obtained instruction
17 sequence; and
18 an execution controlling unit operable to assign (i) the
19 first instruction to the processing elements corresponding to
20 the first-group register files and (ii) the second instruction
21 to the processing elements corresponding to the second-group

22 register files and control the processing elements so that (i)
23 the first and second instructions are executed in parallel, (ii)
24 the processing elements executing the first instruction are
25 employed in parallel for the execution, and (iii) the processing
26 elements executing the second instruction are employed in
27 parallel for the execution.

1 12. The parallel execution processor of Claim 11, wherein
2 the register files are arranged in the register so that
3 the first-group register files and the second-group register
4 files alternate.

1 13. The parallel execution processor of Claim 12, wherein
2 the register files are formed into a plurality of pairs,
3 keeping an order in which the register files are arranged in
4 the register,

5 each of the instructions includes a piece of selection
6 information indicating which piece of data, each processing
7 element should obtain, selecting out of (a) the piece of data
8 stored in the corresponding register file and (b) the piece of
9 data stored in a register file with which the corresponding
10 register file is paired, and

11 each of the processing elements obtains the piece of data
12 to be processed from the register file indicated in each piece

13 of selection information.

1 14. An instruction assigning method for assigning
2 instructions to a plurality of processing elements, comprising:
3 an obtaining step of obtaining (i) a piece of group number
4 information indicating how many groups the processing elements
5 should be formed into and (ii) an instruction sequence including
6 one or more instructions;

7 a decoding step of decoding the obtained instruction
8 sequence;

9 a group forming step of forming the processing elements
10 into as many groups as indicated by the piece of group number
11 information; and

12 an execution controlling step of assigning part or all
13 of the instructions included in the decoded instruction sequence
14 to the groups, so that one group receives one instruction, and
15 controlling the processing elements so that (i) the instructions
16 received by the groups are executed in parallel, and (ii) in
17 each group, all processing elements in the group are employed
18 in parallel for the execution of the received instruction.

1 15. An instruction assigning method for assigning a first
2 instruction and a second instruction to a plurality of
3 processing elements, the instruction assigning method

4 comprising:

5 a storing step of (i) reading as many pieces of data as
6 the number of processing elements, from a memory in which (a)
7 pieces of data to be processed when a first instruction is executed
8 and (b) piece of data to be processed when a second instruction
9 is executed are arranged in an order according to a predetermined
10 rule and (ii) storing the pieces of data, without changing the
11 order, into register files each of which corresponds to a
12 different one of the processing elements;

13 an obtaining step of obtaining an instruction sequence
14 that includes the first instruction and the second instruction;

15 a decoding step of decoding the first instruction and the
16 second instruction included in the obtained instruction
17 sequence; and

18 an execution controlling step of assigning (i) the first
19 instruction to the processing elements corresponding to the
20 register files that each store therein the piece of data to be
21 processed when the first instruction is executed and (ii) the
22 second instruction to the processing elements corresponding to
23 the register files that each store therein the piece of data
24 to be processed when the second instruction is executed, and
25 controlling the processing elements so that (i) the first and
26 the second instructions are executed in parallel, (ii) the
27 processing elements executing the first instruction are employed

28 in parallel for the execution, and (iii) the processing elements
29 executing the second instruction are employed in parallel for
30 the execution.